In the Claims:

1. (Previously presented) A parallel processing apparatus for processing data based on instruction words comprising at least two individual instructions used for controlling at least two respective functional units, said apparatus comprising:

an instruction processor arranged to process a first individual instruction extracted from a first instruction word, and at least a second individual instruction extracted from at least a subsequent second instruction word, as a new single instruction word, the instruction processor further arranged to add predetermined control information to said single instruction word, said control information indicating an allocation of said extracted first and at least second individual instructions to said respective functional units and a sequential order of said first and at least second individual instructions at their respective functional units; and

a program memory arranged to store said single instruction word.

2. (Previously presented) An apparatus according to claim 1, wherein said instruction processor is arranged to extract said first and at least second individual instructions if said first and at least second instruction words each comprise one of predetermined instruction patterns with at least one delay instruction, and to compress said first and at least second instruction words into said single instruction word.

3. (Original) An apparatus according to claim 2, wherein said delay instruction is a null operation.

4. (Cancelled).

5. (Cancelled).

6. (Previously presented) An apparatus according to claim 1, wherein said control information further includes at least one bit added as at least one respective most significant bit to said single instruction word.

7. (Previously presented) An apparatus according to claim 1, wherein said instruction processor arranged to check said control information in an instruction word read from the program memory to re-establish said first and at least second instruction words based on said control information, and to supply said re-established first and at least second instruction words to an instruction decoder.

8. (Previously presented) An apparatus according to claim 1, wherein said instruction processor is arranged to mark all instruction words associated with delay slots and branch targets, and to decide on extraction of said first and at least second individual instructions based on the markings.

9. (Previously presented) An apparatus according to claim 8, wherein said instruction processor is arranged to adjust at least one program memory address based on a decided extraction.

10. (Original) An apparatus according to claim 1, wherein said parallel processing apparatus is a VLIW processor.

11. (Cancelled).

12. (Currently Amended) A method of compressing instruction words each comprising at least two individual instructions used for controlling at least two respective functional units, said method comprising the steps of:

extracting a first individual instruction from a first instruction word;

extracting at least a second individual instruction from at least one subsequent second instruction word;

generating from said first and second individual instructions a new single instruction word;

adding predetermined control information to said single instruction word, said control information indicating an allocation of the extracted first and at least second

individual instructions to said respective functional units and a sequential order of the first and at least second individual instructions at their respective functional units; and

storing said single instruction word.

13. (Previously presented) A computer readable storage medium storing executable instructions which, when loaded into a computer, cause the computer to perform the steps of a compression method according to claim 12.

14. (Previously presented) An apparatus according to claim 1, wherein said new single instruction word further includes a third individual instruction extracted from a subsequent third instruction word.

15. (Previously presented) An apparatus according to claim 14, wherein the predetermined control information of the new single instruction word further indicates at least one of a functional unit allocation of the extracted third individual instruction and a sequential order of the third individual instruction at an associated functional unit.

16. (Previously presented) A method according to claim 12, wherein the added control information further includes at least one bit added as at least one respective most significant bit to said single instruction word.

17. (Previously presented) A method according to claim 12, further comprising:

reading the stored single instruction word;

checking said control information in the read single instruction word;

re-establishing said first and at least second instruction words based on said control information; and

decoding said re-established first and at least second instruction words.